Abstract of the Disclosure

[00132] An effective Electric Wafer Sort (EWS) flow is implemented by expanding the functions of the micro-controller embedded in a FLASH EPROM memory device and of the integrated test structures. The architecture provides for executing test routines internally without involving any external complex or expensive test equipment to control the test program. The processes are executed by the onboard micro-controllers (that may be reading either from an embedded ROM or from a GLOBAL CACHE provided). Managing test routines by an internal process permits the device architecture to be transparent from a tester point of view, by purposely creating a standard interface with a set of defined commands and instructions to be interpreted by the on board microcontroller and internally executed.